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Figure 1: Development Flow

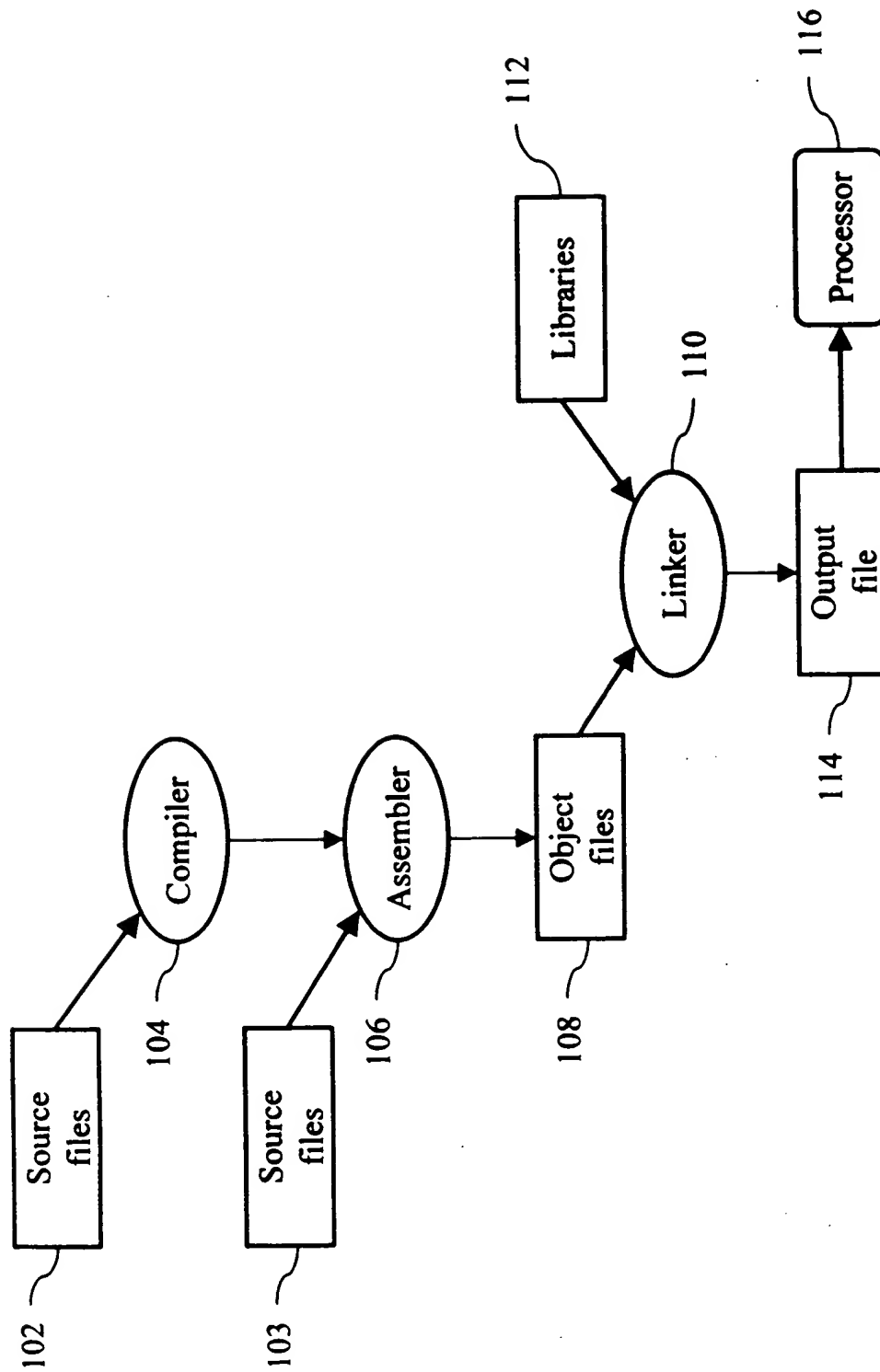


Figure 2A: Typical Linker Apparatus

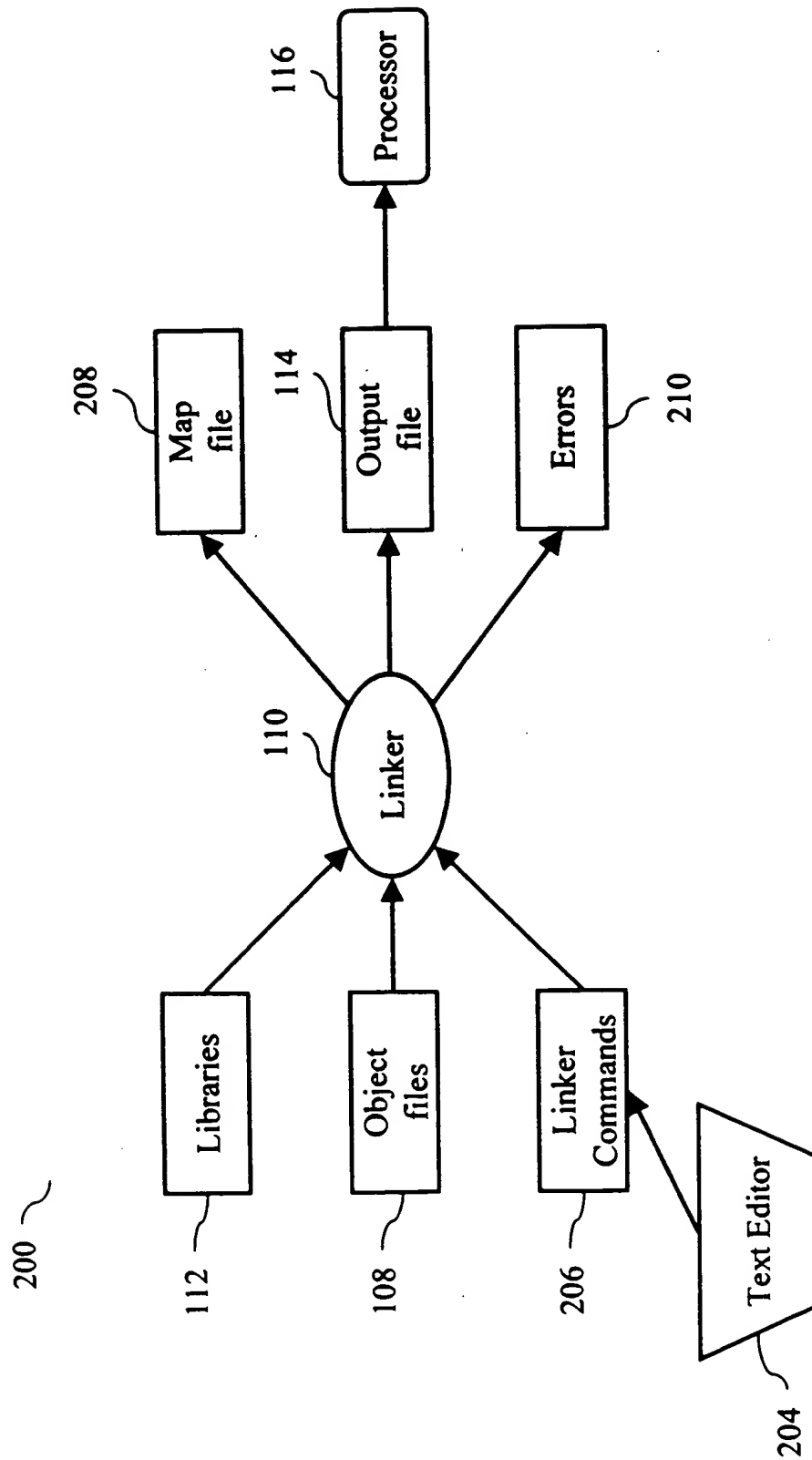


Figure 2B: Typical Linker Method

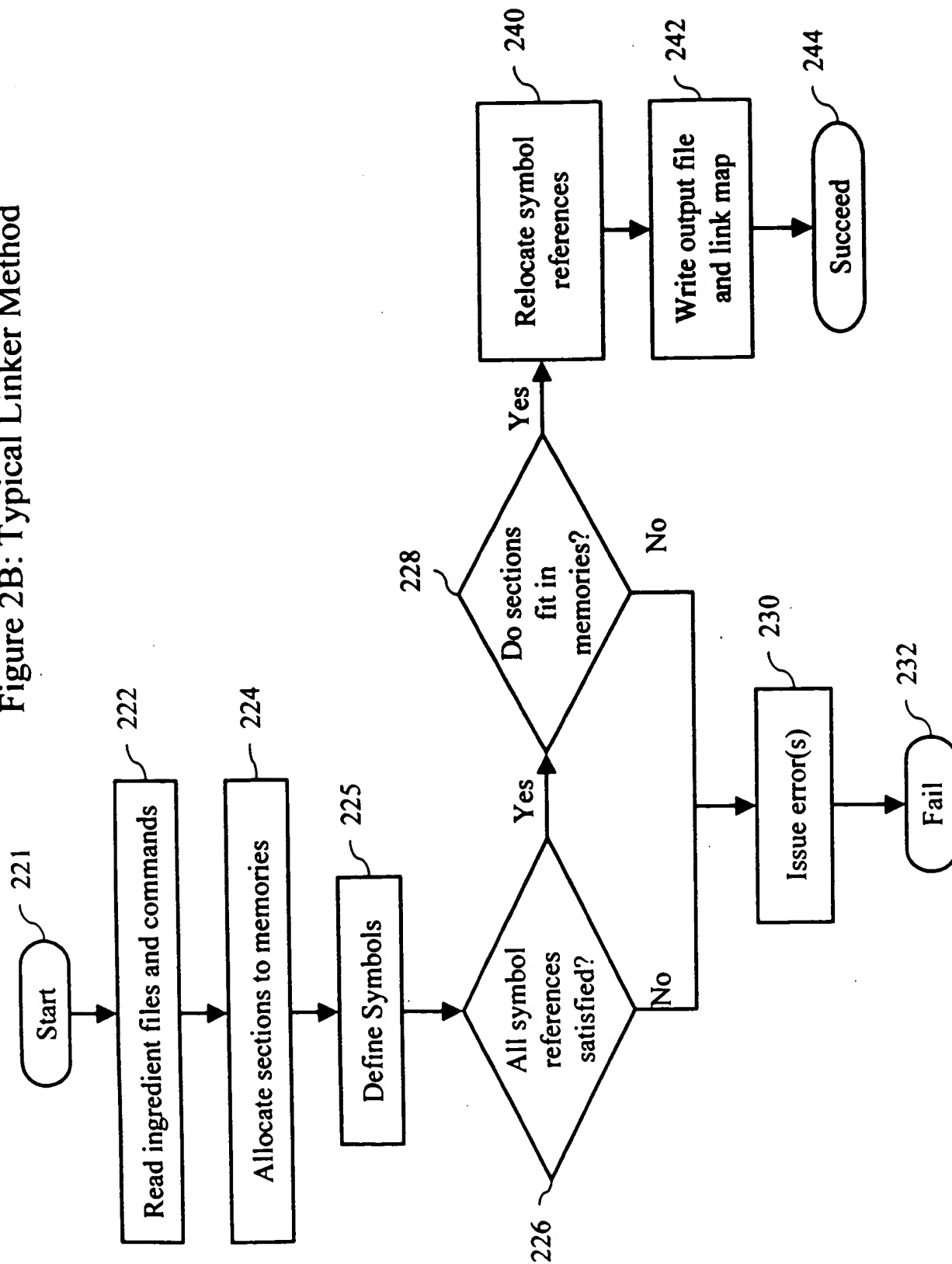


Figure 3: Linker Allocation and Output

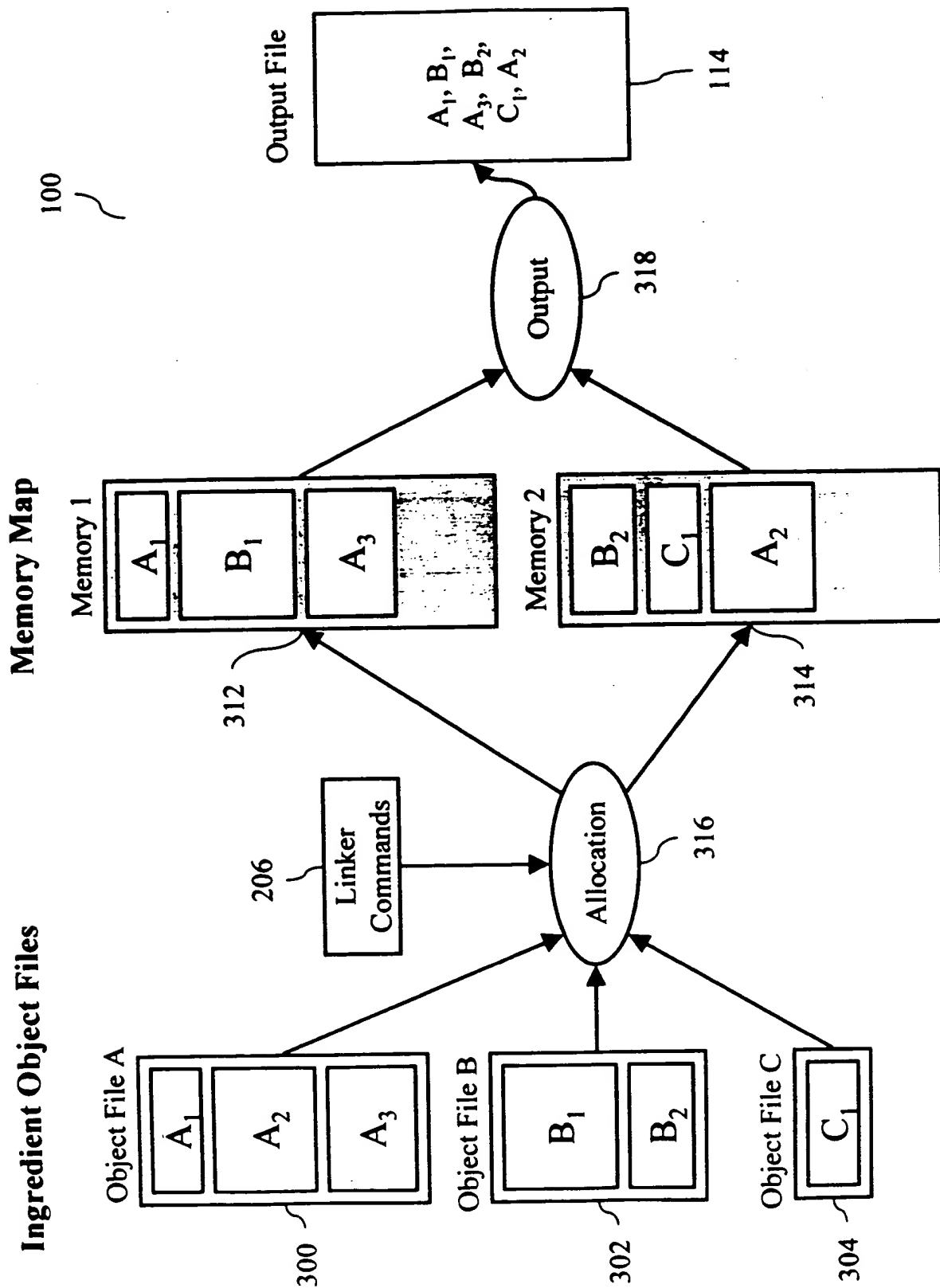
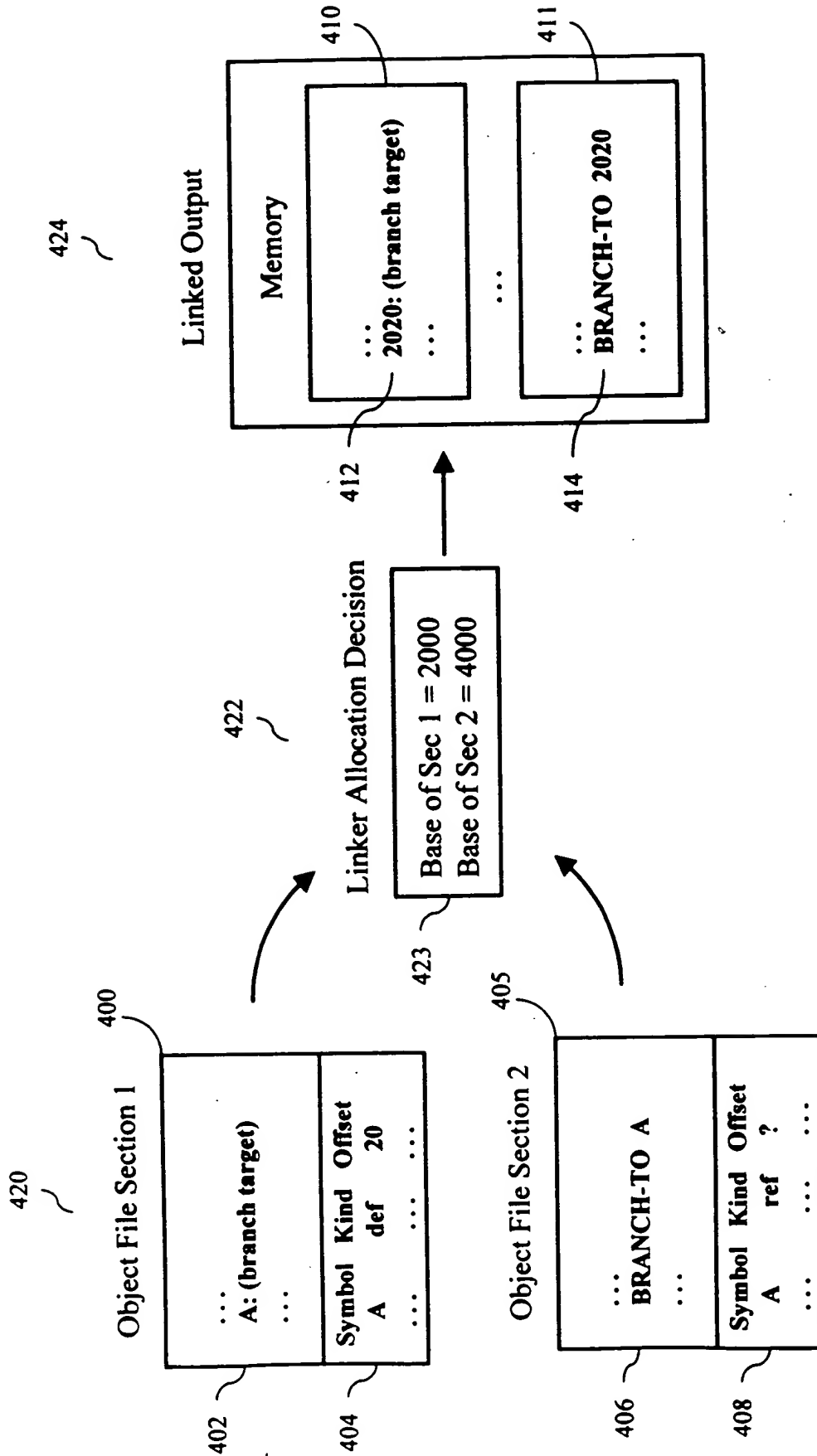


Figure 4: Linker Symbol Resolution



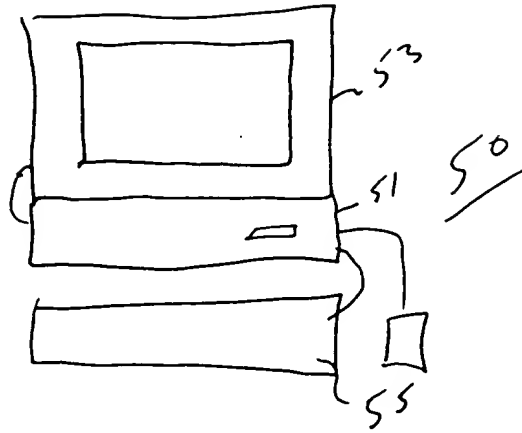


Fig. 5

Figure 6: Original code as produced by compiler or assembler.

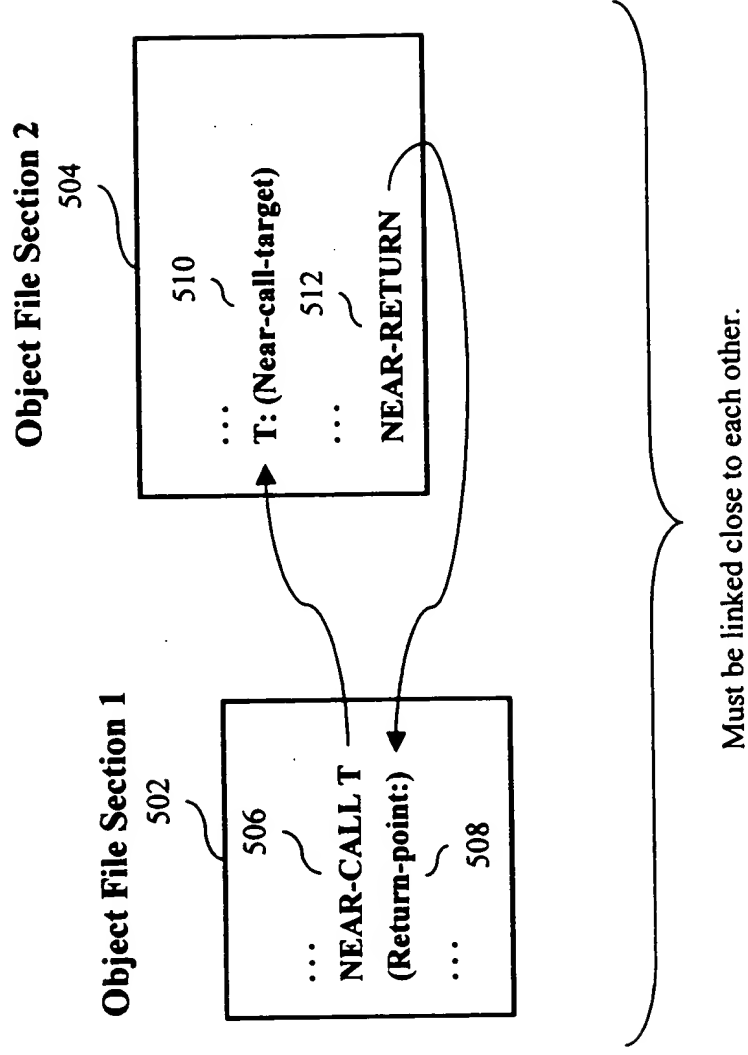


Figure 7: Near call after fixup with single trampoline.

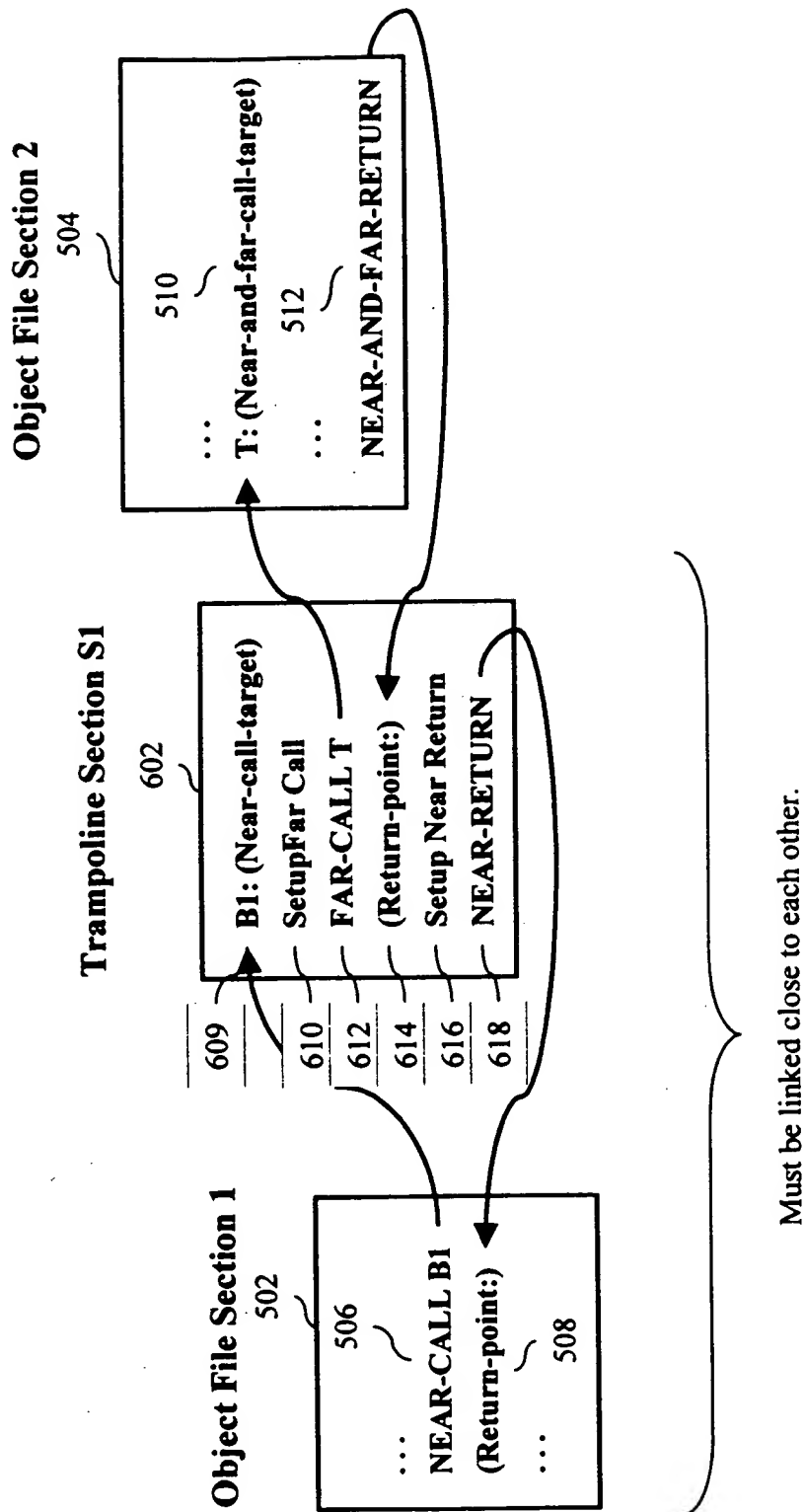
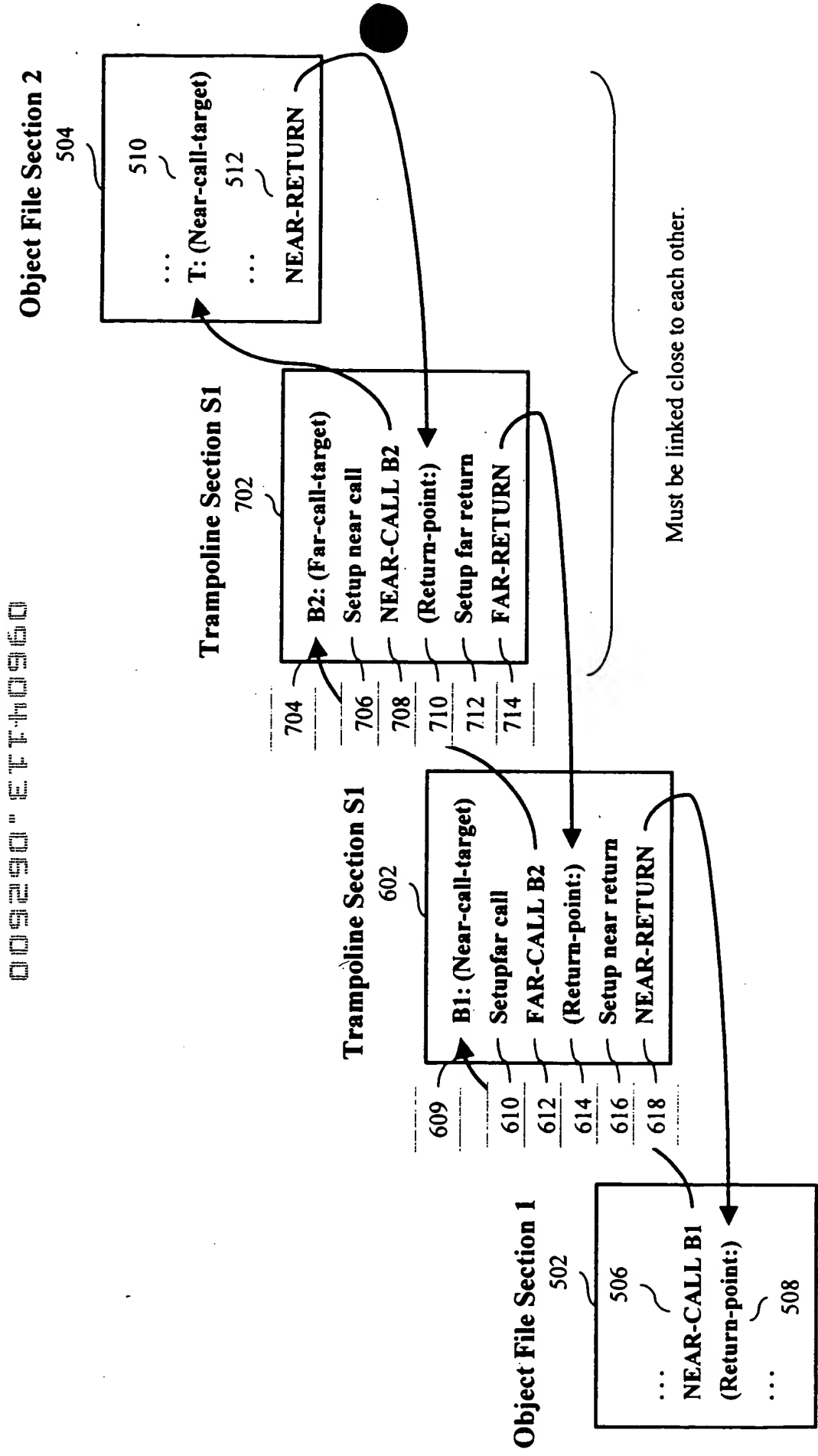


Figure 8: Call after fixup with two trampolines.



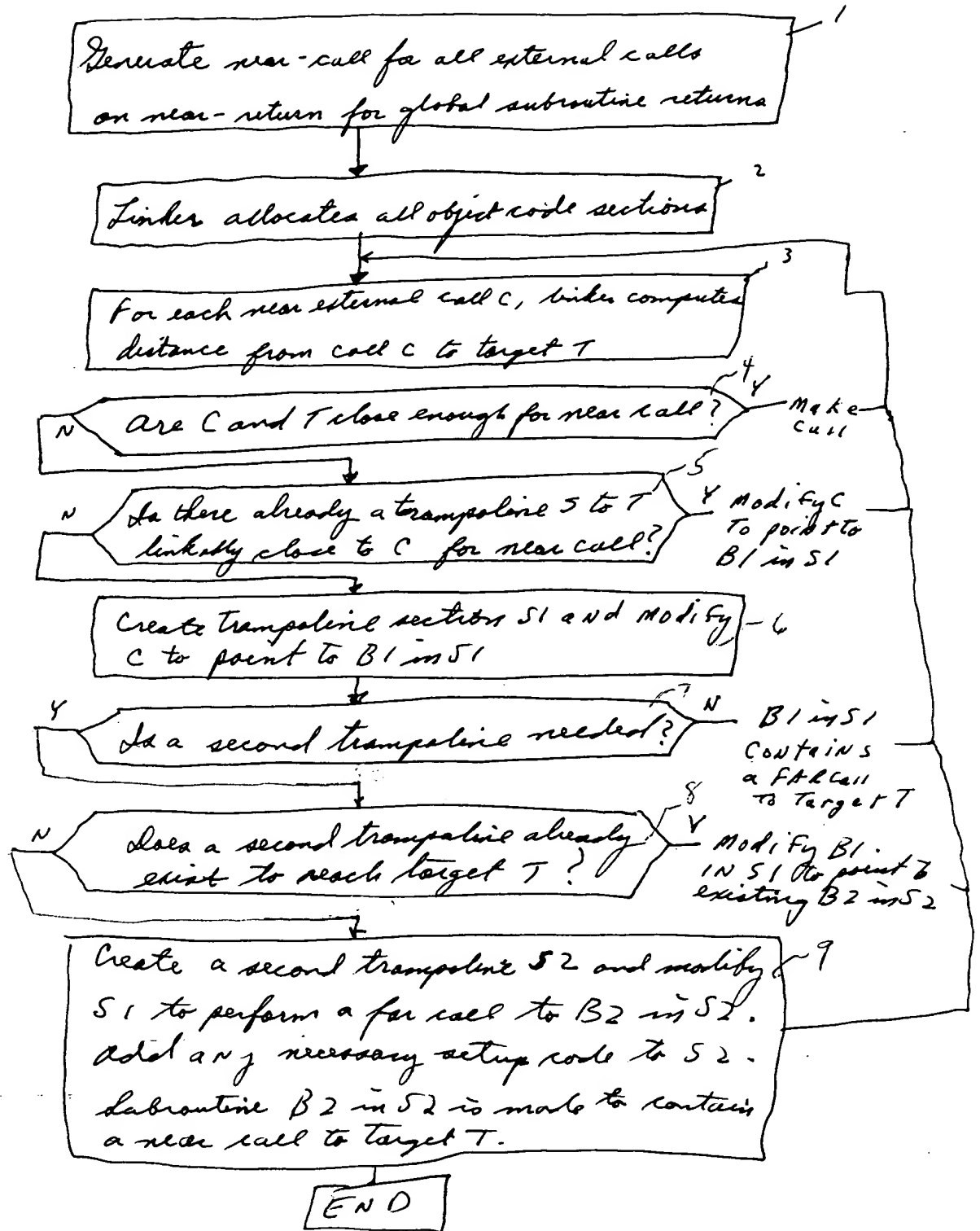


Fig. 9

TRAMPOLINES

Visual Linker [1] Link

ic1

Memory Maps

TMS470R1x

Link-Time Absolute Syms

Need Not Place

ROM

.cmt

.data

.intvecs

.const

470_ROM_out_call

_add2_470_ROM_out_call

_add_470_ROM_out_call

.text

needs_trampoline_text

ic1a\text

.text

_main

RAM

FAR_ROM

ic1c\text

.text

_add2

ic1b\text

.text

_add

load_view

Output Files

All Input Files

icf

INFO

INFO

INFO

INFO

INFO

INFO

INFO

INFO

INFO

INFO

INFO

INFO

Need Not Place

ROM

RAM

FAR_ROM

Need ...

Code ...

Code ...

Code ...

Code ...

Code ...

Code ...

Code ...

Code ...

Code ...

Code ...

Code ...

Code ...

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Code ...

Code ...

Code ...

0000000h

01FFFFFh

05FFFFFFh

F01FFFFFFh

0200000h

0400000h

0800000h

F0000000h

F0200000h

run_view

0008000h

0000000h

0000000h

0000000h

0000000h

0000000h

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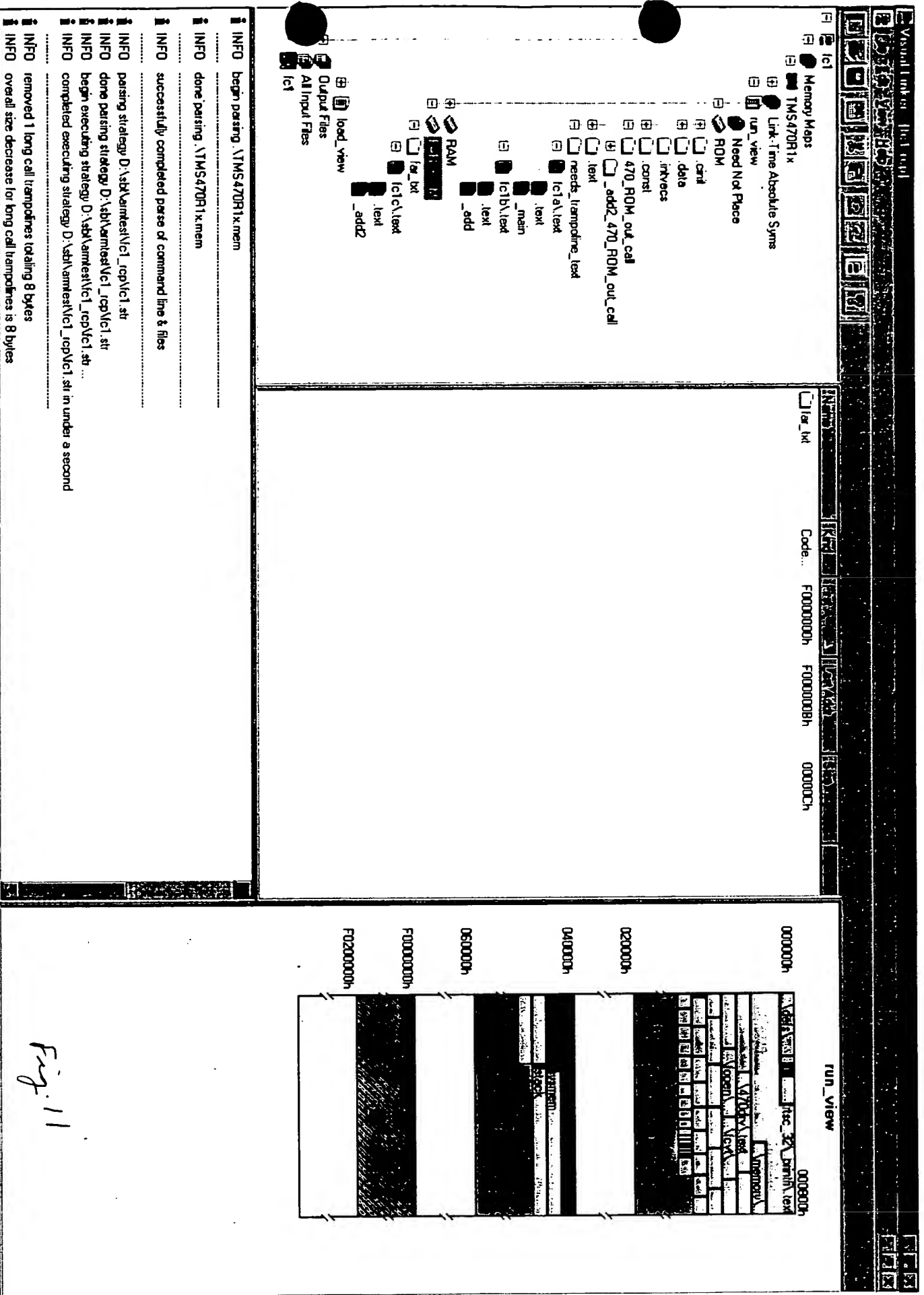
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Fig. 10 (16)

096041.13 . 062600

Fig. 11



0560413 056000